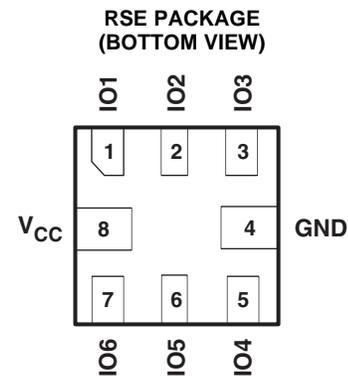


## FEATURES

- ESD Protection Exceeds JESD
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC 61000-4-2 Contact Discharge
  - $\pm 12$ -kV IEC 61000-4-2 Air-Gap Discharge
- Low 1.6-pF IO Capacitance
- 0.9-V to 5.5-V Supply-Voltage Range
- 6-Channel Device
- Space-Saving QFN (RSE) Package

## APPLICATIONS

- USB
- Ethernet
- FireWire
- Video
- Cell Phones
- SVGA Video Connections
- Glucose Meters



## DESCRIPTION/ORDERING INFORMATION

The TPD6E004 is a low-capacitance  $\pm 15$ -kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steers ESD current pulses to  $V_{CC}$  or GND. The TPD6E004 protects against ESD pulses up to  $\pm 15$ -kV Human-Body Model (HBM),  $\pm 8$ -kV Contact Discharge, and  $\pm 12$ -kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a typical 1.6-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

The TPD6E004 is a six-channel ESD structure designed for wthernet and FireWire applications.

The TPD6E004 is available in the RSE package and is specified for  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  operation.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	QFN – RSE 1.5 mm $\times$ 1.5 mm, Pitch = 0.5 mm, Height = 0.55 mm	Reel of 3000	TPD6E004RSER	2V

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



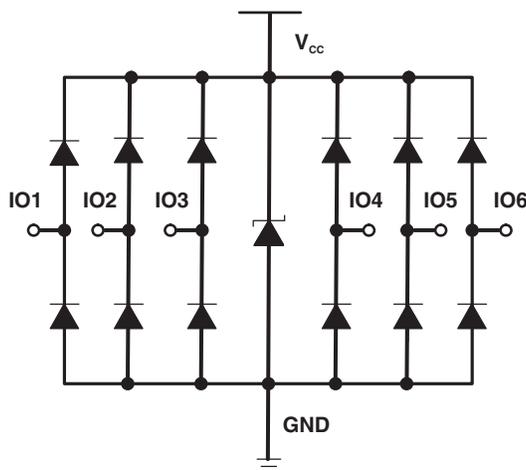
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**TPD6E004**  
**LOW-CAPACITANCE 6-CHANNEL  $\pm 15$ -kV ESD PROTECTION ARRAY**  
**FOR HIGH-SPEED DATA INTERFACES**

SLLS799A—FEBRUARY 2008—REVISED FEBRUARY 2008

**LOGIC BLOCK DIAGRAM**



**PIN DESCRIPTION**

RSE NO.	NAME	FUNCTION
1-3, 5-7	IOx	ESD-protected channel
4	GND	Ground
8	V <sub>CC</sub>	Power-supply input. Bypass V <sub>CC</sub> to GND with a 0.1- $\mu$ F ceramic capacitor.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V <sub>CC</sub>	-0.3	5.5	V
V <sub>IO</sub>	-0.3	V <sub>CC</sub> + 0.3	V
T <sub>stg</sub> Storage temperature range	-65	150	$^{\circ}$ C
T <sub>J</sub> Junction temperature		150	$^{\circ}$ C
Bump temperature (soldering)	Infrared (15 s)	220	$^{\circ}$ C
	Vapor phase (60 s)	215	$^{\circ}$ C
Lead temperature (soldering, 10 s)		300	$^{\circ}$ C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

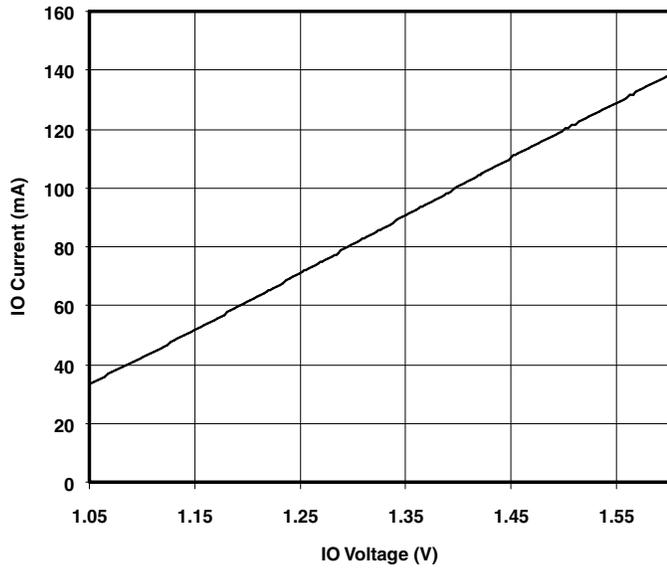
PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{CC}$	Supply voltage		0.9		5.5	V
$I_{CC}$	Supply current				500	nA
$V_F$	Diode forward voltage	$I_F = 1\text{ mA}$		0.8		V
$I_l$	Channel leakage current			±1		nA
$V_{BR}$	Break-down Voltage	$I_l = 10\mu\text{A}$	6		8	V
$C_{I/O}$	Channel input capacitance	$V_{CC} = 5\text{ V}$ , Bias of $V_{CC}/2$ , $f = 10\text{MHz}$		1.6	2	pF

(1) Typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

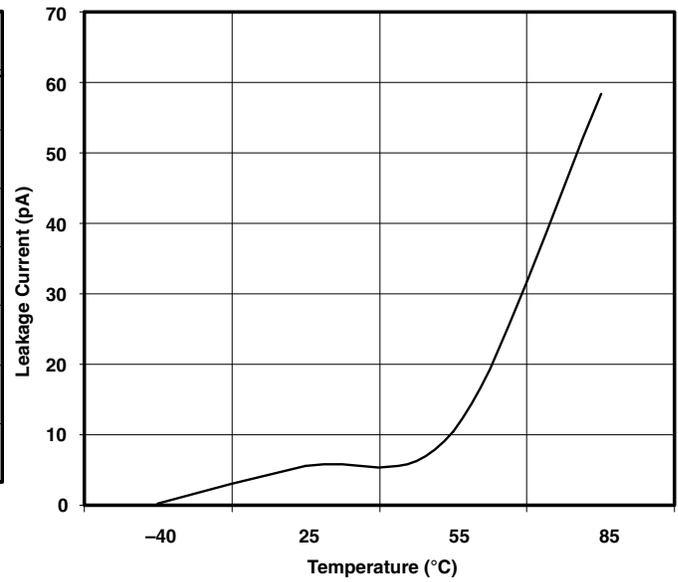
## ESD PROTECTION

PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 Contact Discharge	±8	kV
IEC 61000-4-2 Air-Gap Discharge	±12	kV

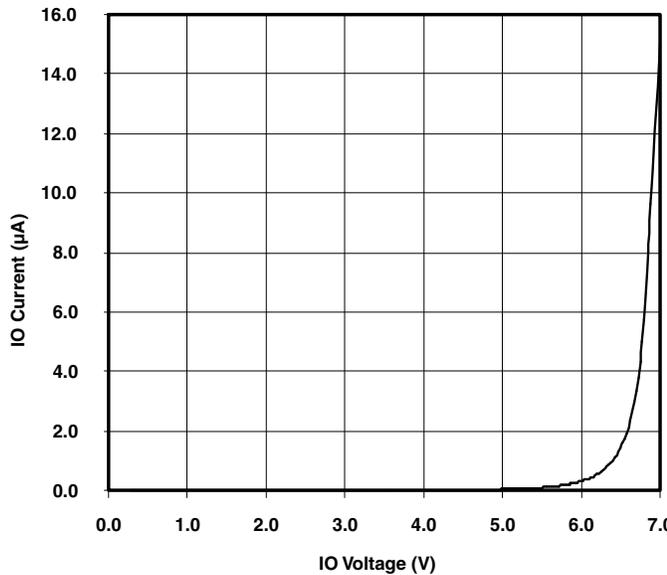
**TYPICAL OPERATING CHARACTERISTICS**



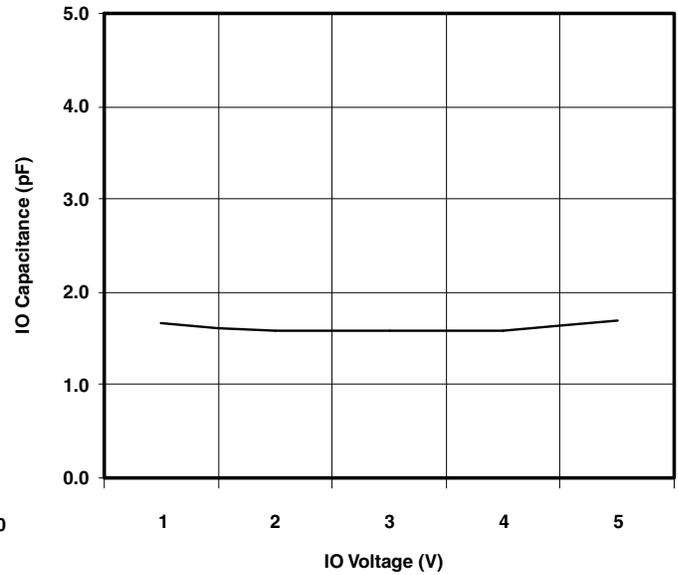
**Figure 1. Forward Diode Voltage (Upper Clamp Diode)**  
( $V_{CC} = 0$  V, DC Sweep Across the IO Pin)



**Figure 2. Leakage Current vs Temperature ( $V_{IO} = 2.5$  V)**



**Figure 3. Reverse Diode Curve Current IO to GND**  
( $V_{CC} = \text{Open}$ )



**Figure 4. IO Capacitance vs Input Voltage**  
( $V_{CC} = 5$  V)

TYPICAL OPERATING CHARACTERISTICS (continued)

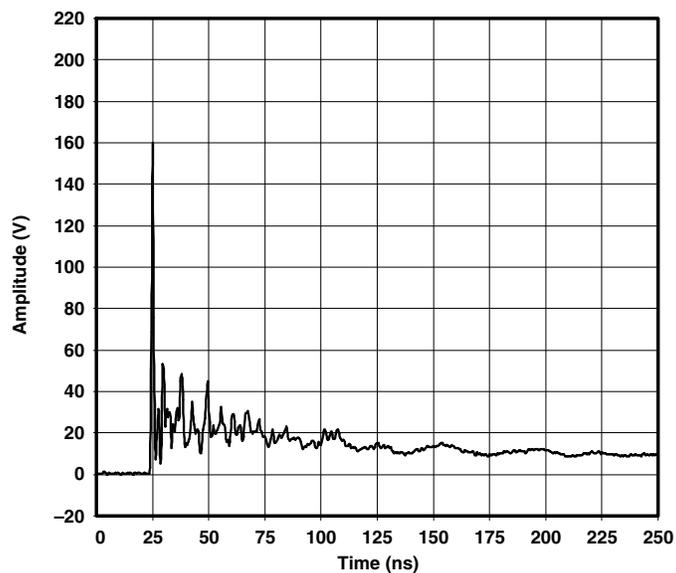
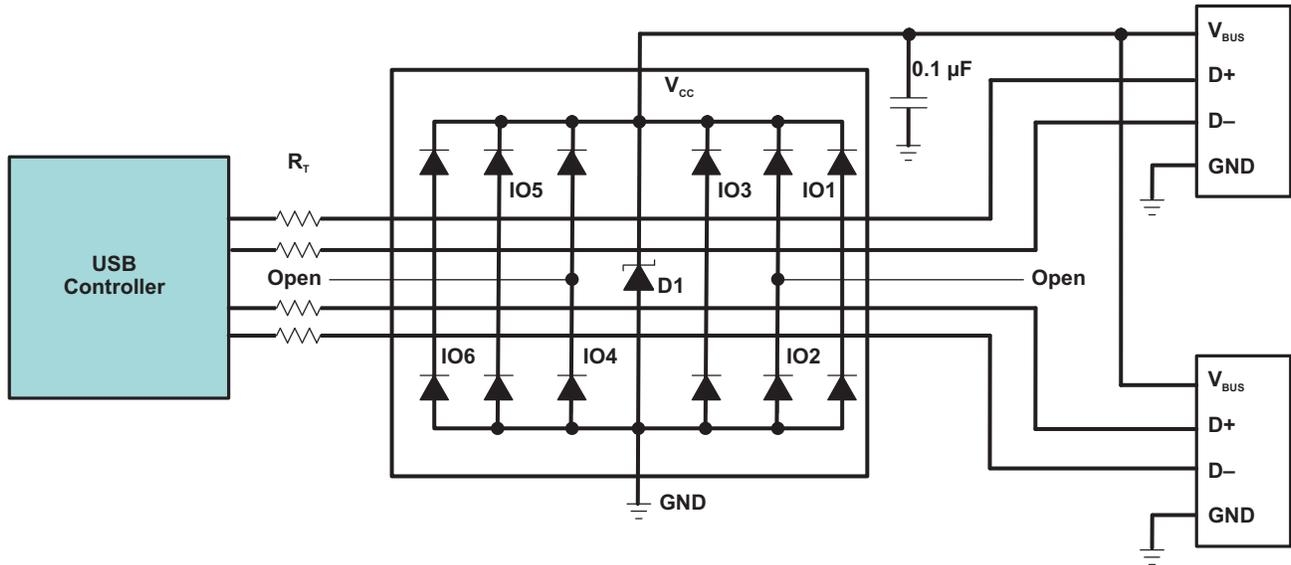


Figure 5. IEC ESD Clamping Waveforms +8-kV Contact,  
Average of 10 Waveforms

**TPD6E004**  
**LOW-CAPACITANCE 6-CHANNEL  $\pm 15$ -kV ESD PROTECTION ARRAY**  
**FOR HIGH-SPEED DATA INTERFACES**

SLLS799A—FEBRUARY 2008—REVISED FEBRUARY 2008

**APPLICATION INFORMATION**



**Detailed Description**

When placed near the connector, the TPD6E004 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD6E004 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/design guidelines should be followed:

1. Place the TPD6E004 solution close to the connector. This allows the TPD6E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1- $\mu F$  capacitor very close to the  $V_{CC}$  pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Make sure that there is enough metallization for the  $V_{CC}$  and GND loop. During normal operation, the TPD6E004 consumes nA leakage current. But during the ESD event,  $V_{CC}$  and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating.
5. The  $V_{CC}$  pin can be connected in two different ways:
  - a. If the  $V_{CC}$  pin is connected to the system power supply (a 0.1- $\mu F$  capacitor at  $V_{CC}$  is recommended for ESD bypass), the TPD6E004 works as a transient voltage suppressor for any signal swing above  $V_{CC} + V_d$ .
  - b. If the  $V_{CC}$  pin is not connected to system power supply (a 0.1- $\mu F$  capacitor is still recommended at the  $V_{CC}$  pin for ESD bypass), the TPD6E004 can tolerate higher signal swing in the range up to  $V_{BR}$ . Note that initially the bypass capacitor is charged by the signals through clamp diode.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD6E004RSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V	<a href="#">Samples</a>
TPD6E004RSERG4	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

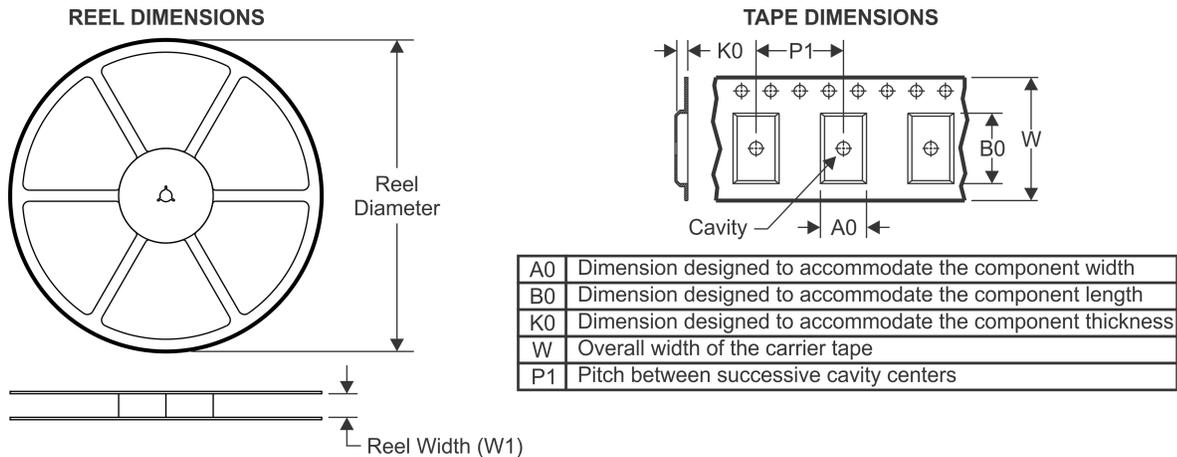
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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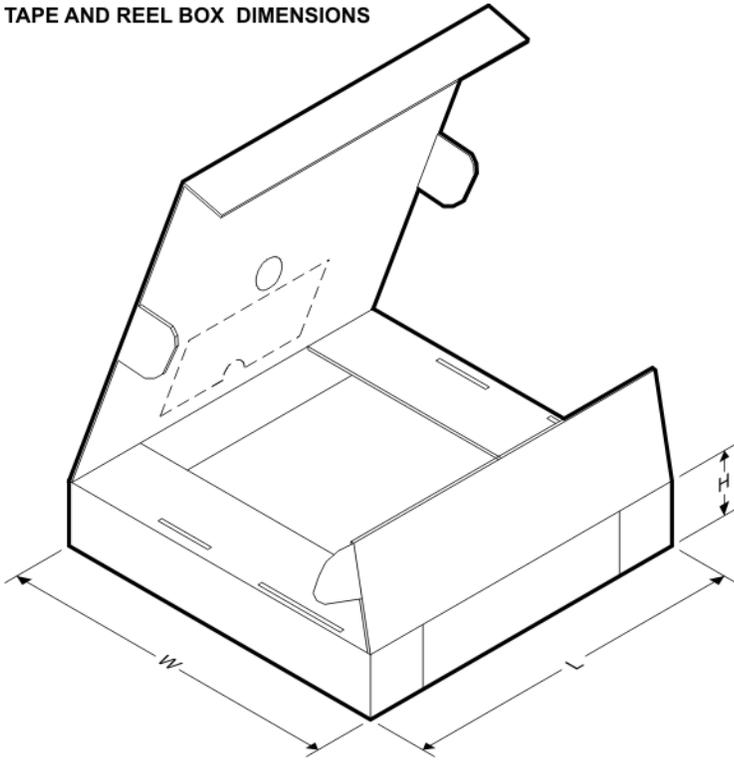
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6E004RSER	UQFN	RSE	8	3000	179.0	8.4	1.7	1.7	0.76	4.0	8.0	Q2
TPD6E004RSER	UQFN	RSE	8	3000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

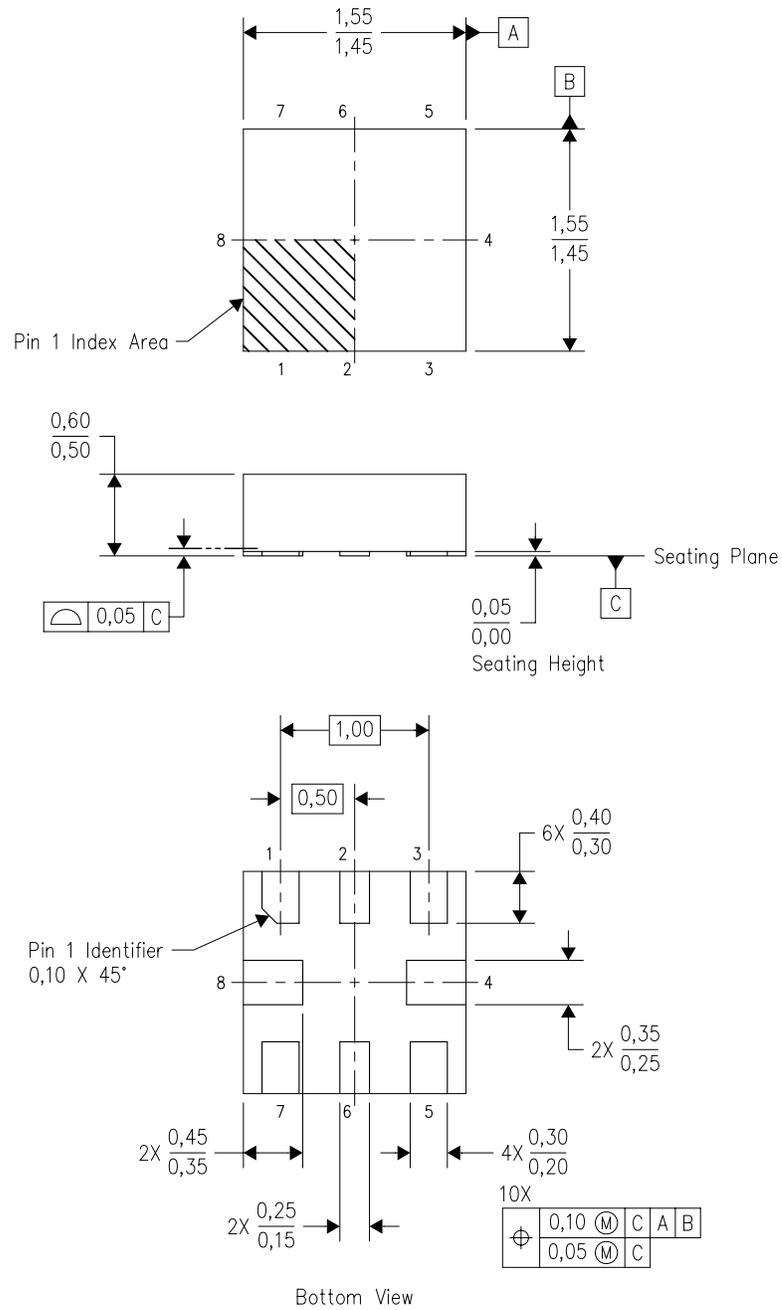


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6E004RSER	UQFN	RSE	8	3000	203.0	203.0	35.0
TPD6E004RSER	UQFN	RSE	8	3000	184.0	184.0	19.0

RSE (S-PUQFN-N8)

PLASTIC QUAD FLATPACK NO-LEAD

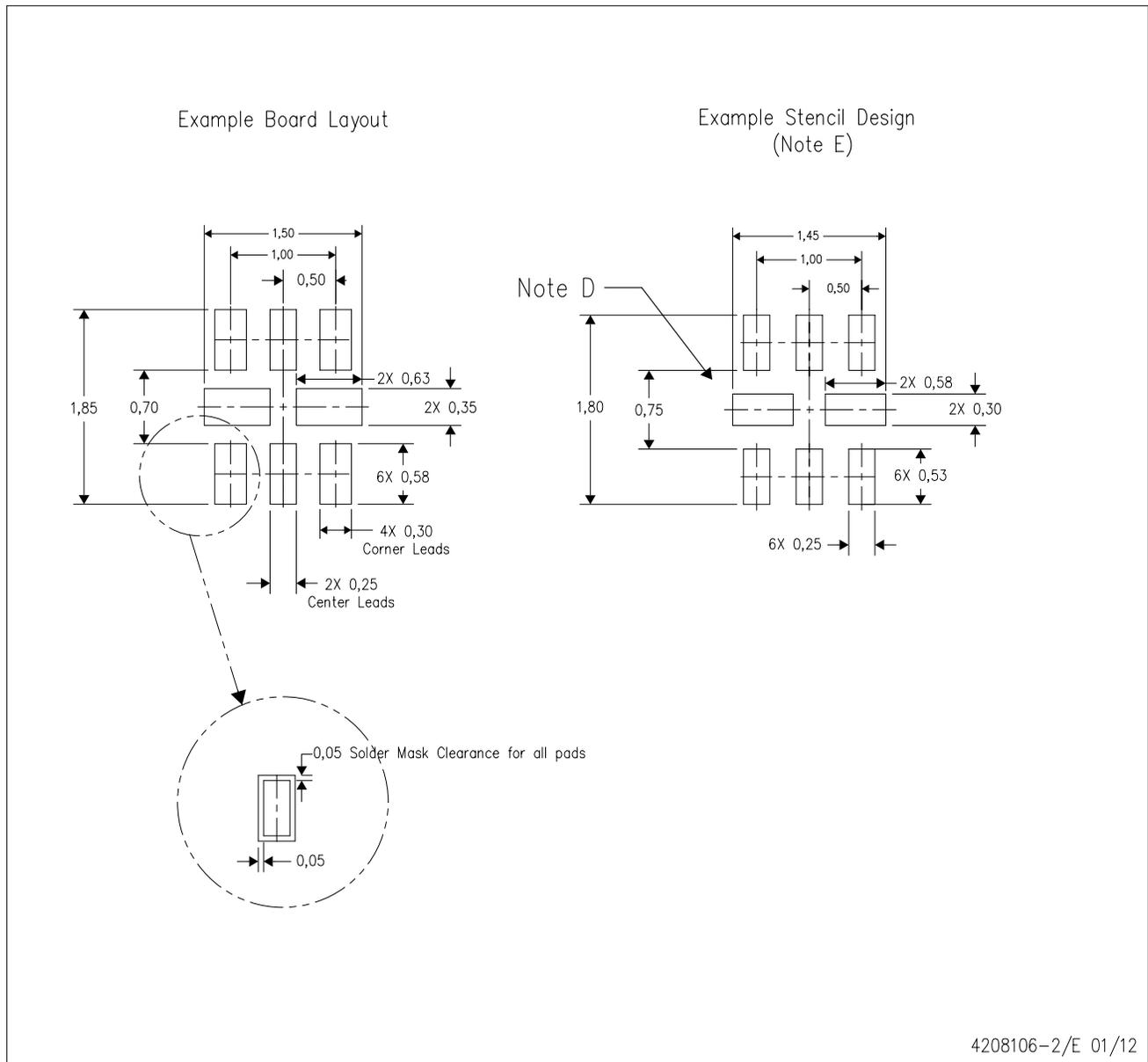


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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. This package complies to JEDEC MO-288 variation UECD.

RSE (S-PUQFN-N8)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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